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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/392,034	GONZALEZ ET AL.	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Prosecution Application

1. The request filed on August 13, 2001 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/392,034 is acceptable and a CPA has been established. An action on the CPA follows.

Claim Objections

2. Claims 2- are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 2, the rounding the top edge of the trench is an inherent result of forming the liner. Thus, claim 2 do not appear to further limits claim 1.

Response to Amendment

3. The amendment filed August 13, 2001 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows:

Claim 1, lines 22-23: "wherein said planarizing is performed in the absent of masking the conformal layer over the isolation trench".

Claim 7, line 20: "planarizing *with a single etch recipe*".

Claim 14, last two lines: "and wherein said selective removing is performed in the absent of masking the conformal second silicon dioxide layer over each said isolation trench".

Claim 42, line 40: "forming *with a single etch recipe*".

Claim 43, last paragraph, lines 4-6: "wherein said planarizing is performed in the absent of masking the conformal second layer over each of said isolation trenches".

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-17, 42 and 43 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "wherein said planarizing is performed in the absent of masking the conformal layer over the isolation trench" and "planarizing *with a single etch recipe*" in the application as filed.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 9, 10, 12, 13, 26, 27, 29 and 30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9 recites the limitation "an etch process using an etch recipe that etches said *first dielectric layer* **faster than** said *conformal layer and said spacer* by a ratio in a range from about 1:1 to about 2:1" in lines 2-4. There is insufficient antecedent basis for this limitation in the claim.

Claims 10, 12, 13, 26, 27, 29 and 30 recite different ratios, which is the first dielectric layer (insulator island 22) is etched **faster than** the conformal layer (isolation film 36) and spacer (spacers 28).

The specification, on another hand, discloses a **completely opposite**: "preferably, planarization will be selective to isolation film 36 (conformal layer), and relatively slightly selective to insulator island 22 (first dielectric layer), such as by a factor of about one half. A first preferred selectivity of an etch recipe used in the inventive method is in range of about 1:1 to about 2:1, selective to isolation film 36 as compared to insulator island 22. (page 14, lines 14-25).

As best understood by examiner, the paragraph discloses the etch rate of the *conformal layer* (trench fill oxide) to be **faster than** the etch rate of the *first dielectric layer* (silicon nitride masking layer).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Omid-Zohoor et al. (U.S. Patent No. 6,184,108).

As best understood by examiner, Omid-Zohoor teaches a method of forming a microelectronic structure as claimed including:

forming an oxide layer (42) upon a semiconductor substrate (40);

forming a first dielectric layer (44) upon the oxide layer;

selectively removing the first dielectric layer to exposed the oxide layer at a plurality of areas (48);

forming a second dielectric layer (50) conformally over the oxide layer and the first dielectric layer;

selectively removing the second dielectric layer to form a plurality of spacers (52) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with the first dielectric layer (44), and is adjacent to an area of the plurality of areas (48);

forming a plurality of isolation trenches (56) extending below the oxide layer into the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the

spacers (52) and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has a top edge;

rounding the top edge of each of the isolation trenches;

filling each the isolation trench with a conformal layer (64), the conformal layer extending above the oxide layer in contact with a corresponding pair of the spacers;

planarizing the conformal layer and each spacer to form therefrom an upper surface for each the isolation trench that is co-planar to the other the upper surfaces;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

With respect to claim 2, the process of Omid-Zohoor further comprising forming a liner (58) upon a sidewall of each isolation trench (56).

With respect to claim 3, the liner (58) of Omid-Zohoor is a thermally grown oxide of the semiconductor substrate.

With respect to claim 4, the liner (58) of Omid-Zohoor comprises deposition of a composition of matter.

With respect to claim 6, the upper surface for each isolation trench of Omid-Zohoor is formed by polishing (CMP).

7. Claims 7 and 11 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Omid-Zohoor '108.

As best understood by examiner, Omid-Zohoor teaches a method of forming a microelectronic structure as claimed including:

forming an oxide layer (42) upon a semiconductor substrate (40);

forming a first dielectric layer (44) upon the oxide layer;

selectively removing the first dielectric layer to exposed the oxide layer at a plurality of areas (48);

forming a second dielectric layer (50) over the oxide layer and the first dielectric layer;

selectively removing the second dielectric layer to form a plurality of spacers (52) from the second dielectric layer, wherein each spacer is situated upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (56) extending below the oxide layer into the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas, and wherein each isolation trench has an edge;

rounding the top edge of each of the isolation trenches;

filling each the isolation trench with a conformal layer (64), the conformal layer extending above the oxide layer in contact with a corresponding pair of the spacers;

planarizing the conformal layer to form therefrom an upper surface for each the isolation trench that is co-planar to the other the upper surfaces, wherein:

material that is electrically insulative extends continuously between and within the plurality of isolation trenches;

the conformal layer and the spacers form the upper surface for each isolation trench, each upper surface being formed from the conformal layer and the spacer and being situated above the oxide layer; and

the first dielectric layer (44) is in contact with at least a pair of the spacers (52)and the oxide layer (42). (See Figs. 3A-M).

With respect to claim 11, the upper surface of each isolation trench of Omid-Zohoor is formed by the steps comprising:

polishing (CMP), wherein the conformal layer (64), the spacers (52) and the first dielectric layer (44) form a planar first upper surface (66); and

an etch that forms a second upper surface, the second upper surface being situated above the pad oxide layer. (See Fig. 3M).

8. Claim 38 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Omid-Zohoor '108.

Omid-Zohoor teaches a method for forming a microelectronic structure as claimed including:

providing a semiconductor substrate (40) having a top surface with an oxide layer (42) thereon;

forming a first layer (44) upon the oxide layer;

forming a plurality of isolation trenches (56) having electrically insulative material (64) extending continuously between and within the plurality of isolation trench, each isolation trench:

having a spacer (52) composed of dielectric material upon the oxide layer (42) in contact with the first layer (44);

extending from an opening thereto at top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second layer (64) filling the isolation trench and extending above the oxide layer in contact with the spacer;

having a top edge and the top edge being rounded; and

having planar upper surface formed from the second layer (64) and the spacer (52) and being situated above the oxide layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers. the second layer, and the plurality of isolation trenches. (See Figs. 3A-M).

9. Claim 41 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Omid-Zohoor '108.

Omid-Zohoor teaches a method of forming a microelectronic structure as claimed including:

providing a semiconductor substrate (40) having a top surface;

forming first and second isolation trenches (56) each:

extending into and being defined by the semiconductor substrate;

having an opening thereto at the top surface of the semiconductor substrate; and

extending below and being centered between a pair of spacers (52) situated above the top surface of the semiconductor substrate; and wherein:

an electrically insulative material (64) extends continuously between and within the first and second isolation trenches; and

a planar surface begins at the first isolation trench and extends continuously to the second isolation trench; and

wherein the microelectronic structure is defined at least in part by the pair of spacers, the electrically insulative material and the first and second isolation trenches. (See Figs. 3A-M).

10. Claim 43 is rejected under 35 U.S.C. 102(e) as being clearly anticipated by Omid-Zohoor (U.S. Patent No. 6,097,072).

As best understood by examiner, Omid-Zohoor teaches a method for forming a microelectronic structure as claimed including:

providing a semiconductor substrate (40) having a top surface with an oxide layer (42) thereon;

forming a first layer (44) upon the oxide layer;

forming a first isolation structure including:

a first spacer (52) composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench (56) extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is

situated on a side of the first isolation trench, and wherein the first isolation trench has a top edge that is rounded;

a second spacer (52) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer (52) composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench (56) extending below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench, and wherein the first isolation trench in the second isolation structure has a top edge that is rounded;

a second spacer (52) composed of a dielectric material upon the oxide layer in contact with the first layer (44), the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a conformal second layer (64), composed of an electrically insulative material, conformally filling the first and second isolation trenches and extending continuously

therebetween and above the oxide layer (42) in contact with the first and second spacers (52) of the respective first and second isolation structures; and

planarizing the conformal second layer (64) and the first and second spacers (52) of the respective first and second isolation structures to form a planar upper surface from the conformal second layer (64) and the first and second spacers (52) of respective first and second isolation structures, and being situated above the oxide layer, wherein the microelectronic structure is defined at least in part by the active area, the second layer, and the first and second isolation trenches. (See Figs. 3A-M).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '108 as applied to claim 1 above and further in view of Poon et al. (U.S. Patent No. 5,387,540).

Omid-Zohoor teaches all of the features of the claim with the exception of forming a doped region below the termination of each isolation trench (56).

However, Poon further teaches forming a doped region (30) below the termination of each isolation trench (22) within the semiconductor substrate (12). (See Fig. 4).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a doped region (30) below the termination of each isolation trench

(360) within the semiconductor substrate (120) of Omid-Zohoor as taught by Poon to provide further electrical isolation effect between circuit components.

12. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '108 as applied to claim 7 above, and further in view of Omid-Zohoor '072.

Omid-Zohoor '108 further teaches removing the oxide (42) upon the completion and the trench isolation structure is then ready for additional fabrication process, such as standard CMOS process.

Thus, Omid-Zohoor '108 teaches all the features of the claim with the exception of explicitly disclosing the formation of the MOS device.

However, Omid-Zohoor '072 teaches the formation of the MOS device following the trench isolation includes:

removing the oxide (340) upon the portion of a surface of the semiconductor substrate (120); and forming a gate oxide layer (380) upon the portion of the semiconductor substrate. (See Fig. 3P).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the gate oxide upon the semiconductor substrate of Omid-Zohoor '108 as taught by Omid-Zohoor '072 form the MOS device.

13. Claims 9, 10, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '108.

As best understood by examiner, Omid-Zohoor teach all of the features of the claim with the exception of explicitly disclosing that the etch rate of the conformal third layer (64) and the spacers (52) being faster than that of the first dielectric layer (344).

The selectivity rate of 1:1 to about 2:1 do not appear to be critical.

The CMP process of Omid-Zohoor '108 has resulted in a planar surface (Fig. 3M). The process of Omid-Zohoor '108 is stop when the silicon nitride 44 is exposed.

Further, it appears that the etch recipe of Omid-Zohoor '108 is at least including the claimed range because the etching results in an upper surface for each the isolation trench that is co-planar to the other the upper surfaces. (See Fig. 3M).

Given the teaching of the reference, it would have been obvious to one having ordinary skill in the art at the time of invention to use any etch recipe which comprises a higher removal rate of the oxide than the nitride layer to form a planar surface because as the polishing reaching the nitride layer, electrical or visual detection should be able to stop the polishing before over etching occurred.

Within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum etch ratio of the layers. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation."

14. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '108 in view of Poon et al. (U.S. Patent No. 5,387,540).

As best understood by examiner, Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (42) upon a semiconductor substrate (40);

forming a silicon nitride layer (44) upon the oxide layer;

selectively removing the silicon nitride layer to exposed the oxide layer at a plurality of areas (48);

forming a first silicon dioxide layer (50) over the oxide layer and the silicon nitride layer;

selectively removing the first silicon dioxide layer to form a plurality of spacers (52) from the first silicon dioxide layer, wherein each spacer is situated upon the oxide layer, is in contact with the silicon nitride layer, and is adjacent to an area of the plurality of areas (48);

forming a plurality of isolation trenches (56) extending below the oxide layer into and terminating within the semiconductor substrate, wherein each isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

forming a liner (58) upon a sidewall (56b) of each isolation trench, the liner extending from an interface thereof with the oxide layer (42) to the termination of the isolation trench within the semiconductor substrate;

rounding the top edge of each of the isolation trenches;

filling each isolation trench (56) with a conformal second silicon dioxide layer (64), the second silicon dioxide layer within each isolation trench extending above the oxide layer in contact with a corresponding pair of the spacers; and

selectively removing the conformal second silicon dioxide layer (64) and the spacers (52) to form an upper surface for each isolation trench that is co-planar to the other upper surfaces and being situated above the pad oxide layer, wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all of the features of the claim with the exception of forming a corresponding electrically active region below the termination of the isolation trenches within the semiconductor substrate.

However, Poon teaches forming a corresponding electrically active region (30) below the termination (26) of the isolation trenches (22) within the semiconductor substrate (12). (See Fig. 4).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form electrically active region below the termination (56a) of the isolation trench (56) of Omid-Zohoor as taught by Poon to further provide electrical isolation between circuit components.

With respect to claim 15, the liner (58a) of Omid-Zohoor is thermally grown oxide of the semiconductor substrate.

With respect to claim 16, the liner (50) of Poon is composed of silicon nitride. (see Fig. 11).

With respect to claim 17, the method of Omid-Zohoor further includes removing the oxide (42) upon the completion and the trench isolation structure is then ready for additional fabrication process, such as standard CMOS process. (Fig. 3N).

Thus, Omid-Zohoor '108 teaches all the features of the claim with the exception of explicitly disclosing the formation of the MOS device.

However, Poon '540 teaches the formation of the MOS device following the trench isolation includes:

removing the oxide (14) upon the portion of a surface of the semiconductor substrate (12); and forming a gate oxide layer (44) upon the portion of the semiconductor substrate. (See Fig. 15).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the gate oxide upon the semiconductor substrate of Omid-Zohoor '108 as taught by Poon form the MOS device.

15. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072.

Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a polysilicon layer upon the oxide layer;

forming a first dielectric layer (344) upon polysilicon layer;

selectively removing the first dielectric layer and the polysilicon layer to expose the oxide layer (340) at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer;

selectively removing the second dielectric layer to form a plurality of spacers (356) from the second dielectric layer, wherein each the spacer is upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer into and terminating within the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each the isolation trench with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers;

planarizing the conformal third layer to form therefrom an upper surface for each the isolation trench that is co-planar to the other the upper surfaces;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches;

wherein planarizing the conformal third layer (364) to form therefrom the upper surface for each the isolation trench that is co-planar to the other the upper surfaces further comprises planarizing the conformal third layer and each the spacer to form therefrom the co-planar upper surfaces; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers. the conformal third liver and the plurality of isolation trenches. (See Figs. 3A-M).

Regarding the removal of the polysilicon layer along with the first dielectric layer to expose the oxide layer, as shown in Fig. 3E, the selective removing of Omid-Zohoor '072 includes removing polysilicon layer to expose the oxide layer (340).

With respect to claim 19, the upper surface of each isolation trench of Omid-Zohoor '072 is formed by CMP.

16. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072, as applied to claim 18 above, and further in view of Lee '316.

Omid-Zohoor '072 teaches all the features of the claim with the exception of forming a doped region below the trench.

However, Lee teaches forming a doped region (26) below the termination of each isolation trench (22) within the semiconductor substrate (12). (See Fig. 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a doped region below the termination of each isolation trench (360) within the semiconductor substrate (120) of Omid-Zohoor as taught by Lee to provide further electrical isolation effect between circuit components.

With respect to claim 21, Lee '316 further teaches forming a liner (50) prior to filling the isolation trench. (See Fig. 15).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the liner (50) upon the sidewall of each isolation trench prior to filling each isolation trench (360) of Omid-Zohoor as taught by Lee to release stress on the trench surface.

With respect to claim 22, the liner (50) of Lee is a thermally grown oxide of the semiconductor substrate (32).

17. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 and Lee '316 as applied to claim 21 above, and further in view of Poon '540.

Omid-Zohoor '072 and Lee '316 teach all of the features of the claim with the exception of forming liner comprises deposition of a composition of matter.

However, Poon teaches forming liner (50) upon sidewall (24) of isolation trench (22) comprises deposition of a composition of matter. (See Fig. 11).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form liner (50) of Lee '316 comprises deposition of a composition of matter as taught by Poon to protect the substrate form further oxidation.

18. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072.

Omid-Zohoor '072 teaches a method of forming a microelectronic structure as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a polysilicon layer upon the oxide layer;

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer and the polysilicon layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer;

selectively removing the second dielectric layer to form a plurality of spacers (356) from the second dielectric layer, wherein each the spacer is upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer into and terminating within the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers;

planarizing the conformal third layer to form therefrom an upper surface for each the isolation trench that is co-planar to the other the upper surfaces;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches;

wherein the upper surface for each the isolation trench is formed from the conformal third layer, the spacers, and the first dielectric layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the conformal third layer, and the plurality of isolation trenches. (See Figs. 3A-M).

Regarding the removal of the polysilicon layer along with the first dielectric layer to expose the oxide layer, as shown in Fig. 3E, the selective removing of Omid-Zohoor '072 includes removing polysilicon layer to expose the oxide layer (340).

19. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072.

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a polysilicon layer upon the oxide layer;

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer and the polysilicon layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer;

selectively removing the second dielectric layer to form a plurality of spacers (356) from the second dielectric layer, wherein each the spacer is upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer into and terminating within the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers;

planarizing the conformal third layer to form therefrom an upper surface for each the isolation trench that is co-planar to the other the upper surfaces;

exposing the oxide layer upon a portion of a surface of the semiconductor substrate;

forming a gate oxide layer (380) upon the portion of the surface of the semiconductor substrate;

forming a layer composed of polysilicon (384) upon the gate oxide layer in contact with a pair of the spacers; and

selectively removing the third layer (364), the spacers (356) and the layer composed of polysilicon to form a portion of at least one of the upper surfaces;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-Q).

Regarding the removal of the polysilicon layer along with the first dielectric layer to expose the oxide layer, as shown in Fig. 3E, the selective removing of Omid-Zohoor '072 includes removing polysilicon layer to expose the oxide layer (340).

20. Claims 26 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072.

As best understood by examiner, Omid-Zohoor '072 teaches a method of forming a microelectronic structure substantially as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a polysilicon layer upon the oxide layer;

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer and the polysilicon layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer;

selectively removing the second dielectric layer to form a plurality of spacers (356) from the second dielectric layer, wherein each the spacer is upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer into and terminating within the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each the isolation trench with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers;

planarizing the conformal third layer by an etch using etch recipe to form therefrom an upper surface for each the isolation trench that is co-planar to the other the upper surfaces;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers. the conformal third liver and the plurality of isolation trenches. (See Figs. 3A-M).

Omid-Zohoor is shown to teach all of the features of the claim with the exception of explicitly disclosing that the etch rate of the conformal third layer (364) and the spacers (356) be faster than that of the first dielectric layer (344).

The selectivity rate of 1:1 to about 2:1 do not appear to be critical.

Further, The CMP process of Omid-Zohoor has resulted in a planar surface (Fig. 3M). The process of Omid-Zohoor '072 is stop when the silicon nitride 344 is exposed.

Further, it appears that the etch recipe of Omid-Zohoor '072 is at least including the claimed range because the etching results in an upper surface for each the isolation trench that is co-planar to the other the upper surfaces. (See Fig. 3M).

Given the teaching of the reference, it would have been obvious to one having ordinary skill in the art at the time of invention to use any etch recipe which comprises a higher removal rate of the oxide than the nitride layer to form a planar surface because as the polishing reaching the nitride layer, electrical or visual detection should be able to stop the polishing before over etching occurred.

Within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum etch ratio of the layers. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation."

Regarding the removal of the polysilicon layer along with the first dielectric layer to expose the oxide layer, as shown in Fig. 3E, the selective removing of Omid-Zohoor '072 includes removing polysilicon layer to expose the oxide layer (340).

With respect to claim 27, the ratio range has been discussed above.

21. Claims 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072.

Omid-Zohoor teaches a method of forming a microelectronic structure as claimed including:

forming an oxide layer (340) upon a semiconductor substrate (120);

forming a polysilicon layer upon the oxide layer;

forming a first dielectric layer (344) upon the polysilicon layer;

selectively removing the first dielectric layer and the polysilicon layer to expose the oxide layer at a plurality of areas;

forming a second dielectric layer (352) conformally over the oxide layer, the polysilicon layer, and the first dielectric layer;

selectively removing the second dielectric layer to form a plurality of spacers (356) from the second dielectric layer, wherein each the spacer is upon the oxide layer, is in contact with the first dielectric layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the oxide layer into and terminating within the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each the isolation trench with a conformal third layer (364), the conformal third layer extending above the oxide layer in contact with a corresponding pair of the spacers;

planarizing the conformal third layer to form therefrom an upper surface for each the isolation trench that is co-planar to the other the upper surfaces;

chemical mechanical planarizing the conformal third layer (364), the spacers and the first dielectric layer (344) to form a planar first upper surface; and

etching to forms a planar second upper surface, the second upper surface being situated above the oxide layer;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-N).

Regarding the removal of the polysilicon layer along with the first dielectric layer to expose the oxide layer, as shown in Fig. 3E, the selective removing of Omid-Zohoor '072 includes removing polysilicon layer to expose the oxide layer (340).

With respect to claims 29 and 30, as best understood by examiner, it appears that the etch ratio of Omid-Zohoor '072 is within the claimed range of the present claim because the etching results in an upper surface for each the isolation trench that is co-planar to the other the upper surfaces. (See Fig. 3M).

The claimed ratios do not appears to be critical.

Within purview of one having ordinary skill in the art, it would have been obvious to determine the optimum etch ratio of the layers. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation.".

22. Claims 31, 32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Lee '316.

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

forming a pad oxide layer (340) upon a semiconductor substrate (120);

forming a polysilicon layer upon the oxide layer;

forming a silicon nitride layer (344) upon the polysilicon layer;

selectively removing the silicon nitride layer and the polysilicon layer to expose the oxide layer at a plurality of areas;

forming a first silicon dioxide layer (352) conformally over the oxide layer and the silicon nitride layer;

selectively removing the first silicon dioxide layer to form a plurality of spacers (356) from the first silicon dioxide layer, wherein each the spacer is upon the pad oxide layer, is in contact with the silicon nitride layer, and is adjacent to an area of the plurality of areas;

forming a plurality of isolation trenches (360) extending below the pad oxide layer into and terminating within the semiconductor substrate, wherein each the isolation trench is adjacent to and below a pair of the spacers and is situated at a corresponding area of the plurality of areas;

filling each isolation trench (360) with a conformal second layer (364), the second layer extending above the oxide layer in contact with a corresponding pair of the spacers; and

planarizing the conformal second layer and each spacer to form therefrom an upper surface for each isolation trench that is co-planar to the other upper surfaces and is situated above the pad oxide layer;

wherein material that is electrically insulative extends continuously between and within the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor '072 is shown to teach all of the features of the claim with the exception of forming the doped region below each isolation trench and forming a liner on the sidewall of the trench.

However, Lee teaches forming a corresponding doped region (26) below the termination trench within the semiconductor substrate (12). (See Fig. 3).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a doped region (26) below the termination of each isolation trench (360) within the semiconductor substrate (120) of Omid-Zohoor '072 as taught by Lee to provide further electrical isolation effect between circuit components.

Additionally, Lee teaches forming a liner (24) upon the sidewall of each isolation trench, extending from an interface thereof with the pad oxide layer (14) to the termination of the isolation trench (22) within the semiconductor substrate (12). (See Fig. 3).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the liner (24) upon the sidewall of each isolation trench prior to filling each isolation trench (360) of Omid-Zohoor as taught by Lee to release stress on the trench surface.

With respect to claim 32, the liner (24) of Lee is thermally grown oxide of the semiconductor substrate, and wherein the conformal second layer (364) of '072 is composed of an electrically insulative material.

With respect to claim 34, the method of Omid-Zohoor further includes:

exposing the pad oxide layer (340) upon a portion of a surface of the semiconductor substrate (120);

forming a gate oxide layer (380) upon the portion of the semiconductor substrate; and

forming a layer (384) composed of polysilicon upon the gate oxide layer (380) in contact with a pair of the spacers; and

selectively removing the layer composed of polysilicon to form a portion of at least one of the upper surface. (See Fig. 3Q).

23. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 and Lee '316 as applied to claim 31 above, and further in view of Poon '540.

Omid-Zohoor '072 and Lee '316 also teaches the conformal second layer (364) is composed of an electrically insulative material.

Thus, Omid-Zohoor '072 and Lee '316 teach all of the features of the claim with the exception of forming liner (24) composed of silicon nitride.

However, Poon teaches forming liner (50) comprises silicon nitride upon the isolation trench (22).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form liner (24) of Omid-Zohoor, in view of Lee '316, comprises silicon nitride (50) as taught by Poon '540 to protect the substrate from further oxidizing.

24. Claims 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '108 in view of Lee '316.

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

providing a semiconductor substrate (40) having a top surface with an oxide layer (42) thereon;

forming a first layer (44) over the semiconductor substrate;

forming a plurality of isolation trenches (56) having electrically insulative material (64) extending continuously between and within the plurality of isolation trenches, each isolation trench:

having a spacer (52) composed of a dielectric material upon the oxide layer in contact with the first layer;

extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the spacer;

having a second layer (64) filling the isolation trench and extending above the oxide layer in contact with the spacer (52);

having a top edge and the top edge being rounded; and

having a planar upper surface (66) formed from the second layer(64) and the spacer (52) and being situated above the oxide layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor '108 is shown to teach all of the features of the claim with the exception of forming an etch mask having a polysilicon layer between the oxide layer (42) and the first layer (44).

However, Lee teaches forming an etch mask comprising a polysilicon layer (36) between the oxide layer (34) and the first layer (38). (See Fig. 6).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the etch mask of Omid-Zohoor having a polysilicon layer between the oxide layer and the first layer as taught by Lee to form an etch selectable layer that is differed form the oxide layer and the first dielectric layer.

With respect to claim 36, Lee '316 further teaches:

doping the semiconductor substrate with a dopant having a first conductivity type;

doping the semiconductor substrate (12) below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of each isolation trench. (See Fig. 3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a doped region below the termination of each isolation trench (60) within the semiconductor substrate (40) of Omid-Zohoor '108 as taught by Lee to provide further electrical isolation effect between circuit components.

With respect to claim 37, the width of the doped trench bottom (26) of Lee '316 is greater than the width of the respective isolation trench. (See Fig. 3).

25. Claims 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '108 as applied to claim 38 above, and further in view of Lee '316.

Omid-Zohoor '108 teaches all of the features of the claim with the exception of doping of the semiconductor substrate.

However, Lee '316 teaches:

doping the semiconductor substrate with a dopant having a first conductivity type;

doping the semiconductor substrate (12) below each isolation trench with a dopant having a second conductivity type opposite the first conductivity type to form a doped trench bottom that is below and in contact with a respective one of each isolation trench. (See Fig. 3).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a doped region (26) below the termination of each isolation trench (60) within the semiconductor substrate (40) of Omid-Zohoor '108 as taught by Lee to provide further electrical isolation effect between circuit components.

With respect to claim 40, the width of the doped trench bottom (26) of Lee '316 is greater than the width of the respective isolation trench. (See Fig. 3).

26. Claim 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Omid-Zohoor '072 in view of Lee '316.

Omid-Zohoor teaches a method of forming a microelectronic structure substantially as claimed including:

providing a semiconductor substrate (120) having a top surface with an oxide layer (340) thereon;

forming a first layer (344) over the semiconductor substrate;

forming a first isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench (360) extending from an opening thereto at the top surface of the semiconductor substrate and below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer, wherein the first spacer is situated on a side of the first isolation trench;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer, the second spacer being situated on a side of the first isolation trench opposite the side of the first spacer;

forming a second isolation structure including:

a first spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer;

a first isolation trench (360) extending below the oxide layer into and terminating within the semiconductor substrate adjacent to and below the first spacer of the second isolation structure, wherein the first spacer of the second isolation structure is situated on a side of the first isolation trench;

a second spacer (356) composed of a dielectric material upon the oxide layer in contact with the first layer and the polysilicon layer, the second spacer of the second isolation structure being situated on a side of the first isolation trench opposite the side of the first spacer of the second isolation structure;

forming an active area located within the semiconductor substrate between the first and second isolation structures;

forming a second layer (364), composed of an electrically insulative material, filling the first and second isolation trenches and extending continuously therebetween and above the oxide

layer in contact with the first and second spacers of the respective first and second isolation structures; and

forming a planar upper surface from the second layer and the first and second spacers of the respective first and second isolation structures, and being situated above the oxide layer; and

wherein the microelectronic structure is defined at least in hart by the active area, the second layer and the first and second isolation trenches. (See Figs. 3A-M).

Thus, Omid-Zohoor is shown to teach all of the features of the claim with the exception of forming a polysilicon layer upon the oxide layer (340).

However, Lee teaches forming a polysilicon layer (36) between the oxide layer (34) and the first dielectric layer (38). (See Fig. 6).

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form a polysilicon layer (36) between the oxide layer (340) and the first dielectric layer (344) of Omid-Zohoor as taught by Lee to form an etch selectable layer that is differed form the oxide layer and the first dielectric layer.

Response to Arguments

27. Applicant's arguments with respect to claims 1-43 have been considered but are moot in view of the new ground(s) of rejection.

Rejection under 35 USC § 102.

Contrary to applicant's contention, the amended portions "planarization that is performed in ***the absence of masking*** of the conformal layer over at least one isolation trench" and

"planarization ***with a single etch recipe***" ***do not*** explicitly have support in the original specification as filed.

Applicant is required to cancel the new matters according to 35 U.S.C. 132.

Rejection under 35 USC § 103(a).

Regarding Lee et al. (U.S. Patent No. 5,229,316), the issue date of Lee, July 20, 1993, is more than one year to any of the commonly own applicants. Therefore, Lee '316 reference is clearly a prior art under 102(b) thus, 103(a) applied.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (703) 305-0575. The examiner can normally be reached on 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (703) 306-2794. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Anh D. Mai
August 24, 2001

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